REMARKS/ARGUMENTS

The Office Action mailed September 24, 2003, has been received and reviewed. Claims 19, 21 through 23 and 25 through 34 currently pending in the application. Claims 19, 21 through 23 and 25 through 34 stand rejected. Applicant has amended claims 19, 21 through 23 and 25 through 34 solely to replace occurrences of "said" with "the" to enhance the language of the claims and not to avoid the prior art or otherwise narrow the scope of the claims. Applicant respectfully requests reconsideration of the application as amended herein and in view of the arguments set forth hereinbelow.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in view of U.S. patent No. 4,377,619 to Schonhorn et al.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Schonhorn et al. (U.S. Patent No. 4,377,619). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of the claims are improper because the references relied upon by the Examiner fail teach or suggest all of the limitations of the presently claimed invention and because there is a lack of motivation to combine the references in the manner suggested by the Examiner.

Independent claim 19 of the presently claimed invention is directed to a method of fabricating a multi-die assembly. The method comprises: providing a substrate including a plurality of conductors; attaching at least one active face-down base die to the substrate in electrical communication with at least some of the plurality of conductors; providing a layer of conductive epoxy adhesive to a back side of the at least one base die; placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive; curing the layer of conductive epoxy adhesive and securing the back side of at least one stack die to the at least one base die; providing a direct electrical path between the at least one stack die and at least one of the plurality of conductors; and *electrically grounding the at least one base die via the layer of electrically conductive epoxy adhesive and the at least one stack die.*

The Examiner cites Yamauchi as disclosing a method of fabricating a multi-die assembly which comprises: providing a substrate (1) including a plurality of conductors (3); attaching at least one active face down base die to the substrate in electrical communication with at least some of the plurality of conductors; providing a layer of adhesive to a back side of the at least one base die; placing a back side of at least one active face up stack die on the layer of adhesive; securing the back side of at least one stack die to the at least one base die; providing a direct electrical path between the at least one stack die and at least one of the plurality of conductors, and electrically grounding at least one base die via the adhesive and at least one stack die. The Examiner notes that Yamauchi fails to disclose the adhesive is the conductive epoxy adhesive and curing the layer of conductive epoxy adhesive.

The Examiner then cites Schonhorn as disclosing a semiconductor device which comprises: a layer of conductive epoxy adhesive on the substrate; placing a chip on the layer of conductive epoxy adhesive; and curing the layer of conductive epoxy adhesive. The Examiner then concludes that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamauchi to prevent metal migration and to secure more firmly the chip to the substrate, as shown by Schonhorn et al." (Office Action, page 3). Applications respectfully traverse the rejection of claim 19.

Applicant submits that, contrary to the Examiner's assertion, Yamauchi fails to teach or suggest *electrically grounding the at least one base die via the layer of electrically conductive epoxy adhesive and the at least one stack die.*

Considering Yamauchi, the entire translated disclosure thereof Yamauchi includes the following:

> **PURPOSE**: To increase a mounting rate of TAB chips on a printed board by piling up at least two TAB chips an then by mounting these chips on the printed board.
>
> **CONSTITUTION**: At least two TAB chips 2a, 2a are joined with an adhesive 7 wit h end faces having no bump 3 faced each other. The bumps 3 are located on an upper and a lower end face of the TAB chip laminated body 2 and then the TAB chip laminated bodies 2 are piled up. Next, the bumps 3 of the lower TAB chip 2a are joined with a printed board 1 with solder 4. Meanwhile, the bumps 3 of the upper TAB chip 2 are connected with one end of wire leads 6 and the other end of the wire leads is joined to a pad of the printed board 1. By this method, a mounting rate on the printed board 1 can be increased and a TAB chip mounting area can be reduced substantially. (Yamauchi, cover page).

Nowhere in the *Purpose* or *Constitution* does Yamauchi teach or suggest *electrically grounding the at least one base die via a layer of electrically conductive epoxy adhesive and the at least one stack die.* Nor does Schonhorn teach or suggest such subject matter.

Moreover, Applicant submits that there is a lack of motivation to combine the teachings of Yamauchi with Schonhorn. Schonhorn discloses the use of a layer of polymer to prevent either 1) the spreading or bleeding of a liquid on a solid surface or, 2) metal migration from occurring between conductors deposited on a surface of a substrate. The Examiner particularly cites col. 6, lines 1 through 7 to demonstrate the use of a conductive epoxy in association with a semiconductor device. It is noted, however, that the disclosure of conductive epoxy is in

connection with the prevention of the spreading of liquid on a solid surface. In this context, the conductive epoxy adhesive is placed between a semiconductor device 14 and the metallizing layer 11 of a substrate 10. More particularly, with respect to such an embodiment, Schonhorn states that an "example of such an application is the prevention of bleeding of uncured metal-filled adhesive used to bond IC chips to a *metallized substrate*, e.g., a metallized ceramic." (Col. 5, lines 23-26, emphasis added). Thus, Schonhorn only discloses the use of conductive epoxy between a semiconductor device and a metallized substrate. There is no teaching or suggestion that the conductive epoxy should be used between the backs of two semiconductor devices in a stacked assembly.

Furthermore, while the Examiner states that the motivation to use the conductive epoxy of Schonhorn is to "prevent metal migration and to secure more firmly the chip to the substrate," (Office Action, page 3) Applicant notes that Schonhorn fails to teach the use of conductive epoxy for the prevention of metal migration. Rather, a polymer layer having specified material properties is used to prevent metal migration. A similar polymer layer is used to prevent the undue spreading or bleeding *of the conductive epoxy* when used on the metallized substrate.

Moreover, Applicant submits that a motivation of increasing the securement of the semiconductor device to the substrate is improper since, in claim 19 of the presently claimed invention, the conductive epoxy is placed between the base die and the at least one stack die, not between a die and a metallized substrate. As such, there is clearly a lack of motivation to combine the references of Yamauchi with Schonhorn in the manner suggested by the Examiner.

Failing to teach or suggest all the limitations of claim 19, and lacking motivation to combine the references relied upon by the Examiner, Applicant submits that claim 19 is allowable over Yamauchi and Schonhorn and respectfully request reconsideration and allowance thereof.

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in view of U.S. Patent No. 4,377,619 to Schonhorn et al. and further in view of U.S. Patent No. 5,323,060 to Fogal et al.

Claims 21 through 23, 25 through 29 and 33 through 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Schonhorn et al. (U.S. Patent No.4,377,619) and further in view of Fogal et al. (U.S. Patent No. 5,323,060). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant notes that claims 21-23, 25-29 and 33-34 are each dependent from claim 19 either directly or by way of intervening claims. The Examiner relies on Yamauchi and Schonhorn as rendering obvious claim 19, as discussed hereinabove. The Examiner relies on Fogal as teaching a multi-chip semiconductor comprising: at least another stack die (54) electrically connected to the plurality of substrate conductors and attached to the at least one stack die; a discrete component; and bond wires coupling the various components. The Examiner concludes that it "would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamauchi and Schonhorn et al. to provide additional necessary components." (Office Action, page 4). Applicant respectfully traverses this rejection.

As set forth above, Yamauchi and Schonhorn fail to teach or suggest providing a layer of conductive epoxy adhesive to a back side of the at least one base die; placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive; and *electrically grounding the at least one base die via said layer of electrically conductive epoxy adhesive and the at least one stack die.* Additionally, as set forth above, there is a lack of motivation to combine Yamauchi with Schonhorn in the manner suggested by the Examiner.

Applicant further submits that Fogal fails to teach or suggest the subject matter of providing a layer of conductive epoxy adhesive to a back side of the at least one base die; placing a back side of at least one active face-up stack die on the layer of conductive epoxy adhesive; and electrically grounding the at least one base die via said layer of electrically conductive epoxy adhesive and the at least one stack die.

Indeed, Applicant submits that Fogal teaches away from claim 19 of the presently claimed invention in that Fogal expressly teaches that the "[a]dhesive 38 preferably comprises an electrically *insulating* material" (col. 3, lines 8-9, emphasis added). Applicant, therefore, submits that the teachings of Fogal and the teachings of Schonhorn are incompatible inasmuch as Schonhorn teaches the use of an electrically *conductive* adhesive and Fogal teaches the use of an electrical *insulating* adhesive. More importantly, with regard to use of an insulating adhesive, Fogal expressly teaches away from the presently claimed invention.

Applicant further submits that there is a lack of motivation to combine the teachings of Fogal with those of Yamauchi. For example, Yamauchi teaches back-to-back arrangements of the semiconductor dies while Fogal teaches face-to-back arrangements of semiconductor die with no apparent suggestion in either of such references that the teachings of one are applicable to the other.

Applicant, therefore, submits that claims 21-23, 25-29, 33 and 34 are allowable over Yamauchi, Schonhorn, and Fogal, either considered individually or in combination, and respectfully requests reconsideration and allowance of the same.

Obviousness Rejection Based on Japanese Patent No. 5-13665 to Yamauchi in view of U.S. Patent No. 4,377,619 to Schonhorn et al. and U.S. Patent No. 5,323,060 to Fogal et al. and further in view of U.S. Patent No. 5,399,898 to Rostoker

Claims 30 through 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamauchi (Japanese Patent No. 5-13665) in view of Schonhorn et al. (U.S. Patent No.4,377,619) and Fogal et al. (U.S. Patent No. 5,323,060) and further in view of Rostoker (U.S. Patent No. 5,399,898. Applicant respectfully traverses this rejection, as hereinafter set forth.

Each of claims 30-32 depend from claim 19 either directly or through intervening claims. The Examiner relies on the combination of Yamauchi, Schonhorn and Fogal as discussed herein above. The Examiner cites Rostoker as teaching least two active face down base dice and at least one stack die bridging the two base dice. The Examiner concludes that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Yamauchi, Schonhorn et al., an Fogal et al. to provide a

greater power dissipation and a natural convection cooling channel as shown by Rostoker." (Office Action, pages 4 and 5). Applicant respectfully disagrees.

As set forth above, Yamauchi, Schonhorn and Fogal clearly fail to teach or suggest all of the subject matter of the presently claimed invention as set forth in independent claim 19. Particularly, Yamauchi, Schonhorn and Fogal fail to teach or suggest providing a layer of electrically conductive adhesive and grounding the base stack die through the layer of conductive epoxy adhesive. Applicant further submits that Rostoker fails to teach or suggest such subject matter.

Additionally, Applicant submits that there is a lack of motivation to combine the teachings of the references relied upon by the Examiner. As noted above, there is a lack of motivation to provide the conductive adhesive of Schonhorn between the two TAB chips of Yamauchi. Furthermore, as noted above, there is a lack of motivation to combine Fogal with Schonhorn since Fogal teaches the use of electrically *insulating* adhesive while Schonhorn teaches the use of electrically *conductive* adhesive. Additionally, Yamauchi teaches back-to-back arrangements of the semiconductor dies while Rostoker teaches face-to-face arrangements of semiconductor die with no apparent suggestion in any of the references that the teachings of one are applicable to the other.

Moreover, with respect to claims 31 and 32, while the Examiner points to FIG. 4A of Rostoker as teaching the subject matter of bridging two base die with a stack die, Applicant submits that one of ordinary skill in the art would lack motivation to combine such a teaching with Yamauchi. Rostoker explicitly states that such an embodiment requires increased substrate surface area (see, e.g., col. 15, lines 9-11) thereby teaching away from Yamauchi which states that its disclosed arrangement is desirable because it substantially *reduces* mounting area.

Applicant, therefore, submits that claims 30-32 are allowable over Yamauchi, Schonhorn, Fogal and Rostoker, either considered individually or in combination, and respectfully requests reconsideration and allowance of the same.

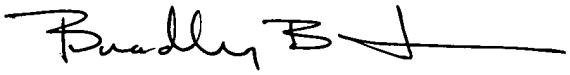
ENTRY OF AMENDMENTS

The amendments to claims 19, 21 through 23 and 25 through 34 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 19, 21 through 23 and 25 through 34 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Bradley B. Jensen
Registration No. 46,801
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: December 3, 2003
BBJ/jml:djp

Document in ProLaw